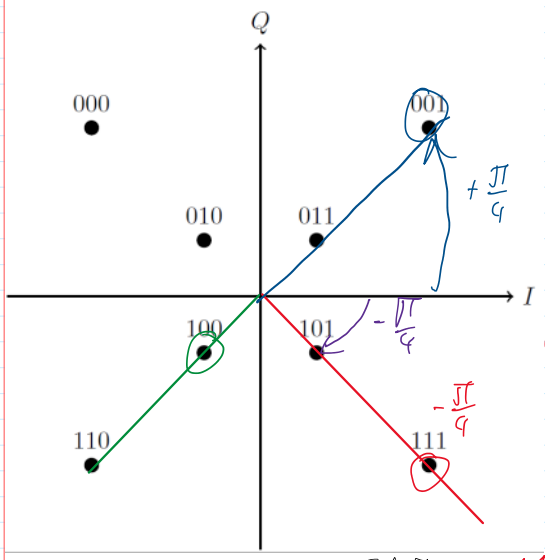
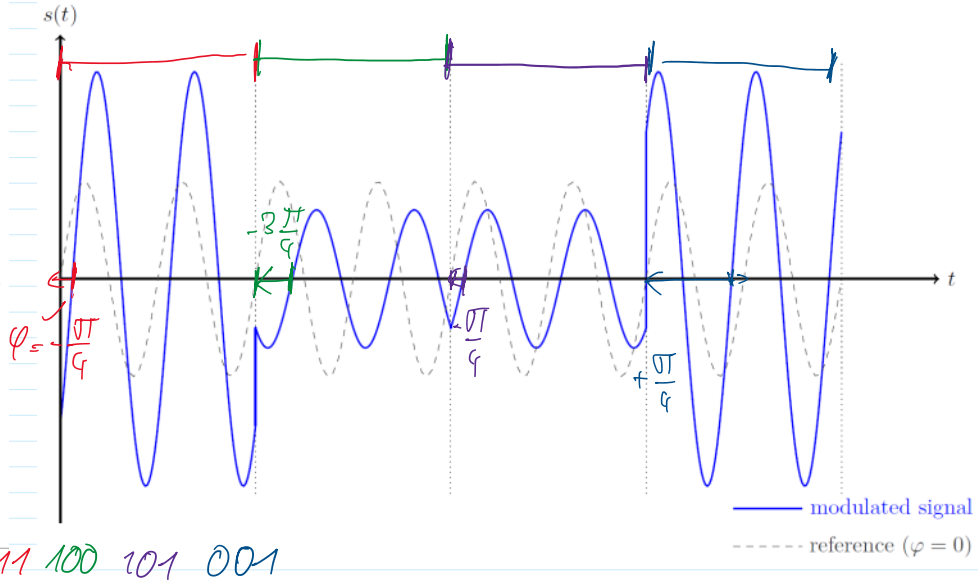
Exercise 1 - Work

Sonntag, 1. Mai 2022 19:22

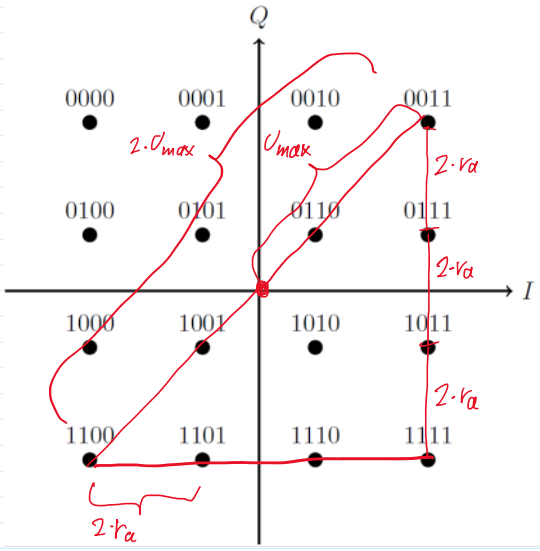
TASK 1 C




Bit-Stream: 111 100 101 001

TASK 1 D




$(2 \cdot U_{max})^2 = (2 \cdot 3 \cdot r_a)^2 \cdot 2$

$4 \cdot U_{max}^2 = (6 \cdot r_a)^2 \cdot 2 \quad |:2$

$2 \cdot U_{max}^2 = 6^2 \cdot r_a^2$

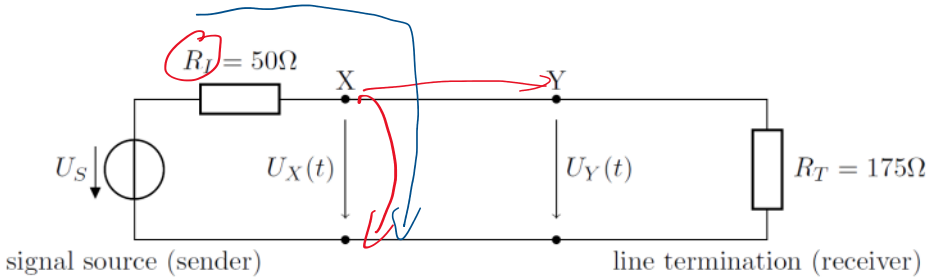
$2 \cdot 72V^2 = 36 \cdot r_a^2 \quad |:36$

$2 \cdot 2V^2 = r_a^2 \quad |\sqrt{}$

$2V = r_a$

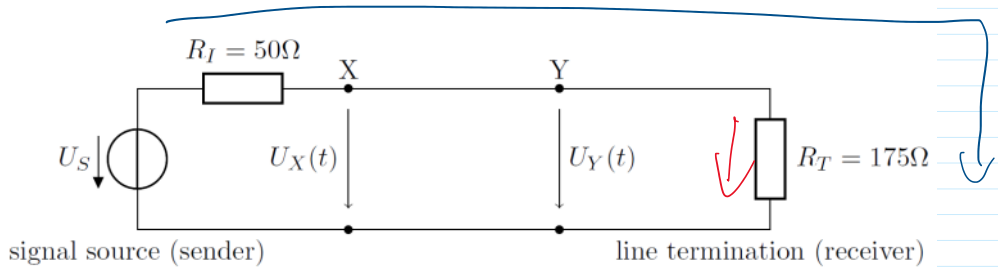
We want U_max as the distance to the outermost points (0011, 0000, 1100, 1111) because this allows us to send data with the highest possible voltage, resulting an better SNR.

TASK 2 A



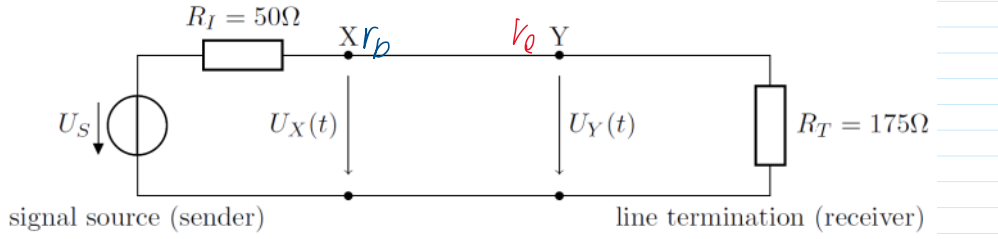

$U_x(0) = \frac{Z_0}{R_I + Z_0} \cdot U_S(0) = \frac{75\Omega}{75\Omega + 50\Omega} \cdot 5V = 3V$

TASK 2 B

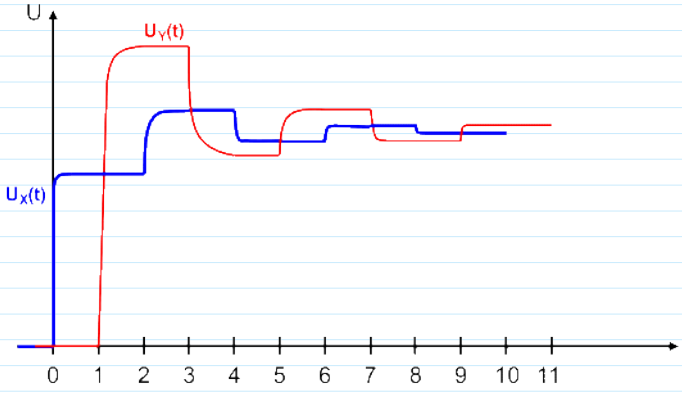



$$U_X(\infty) = \frac{R_T}{R_I + R_T} \cdot U_S(\infty) = \frac{175\Omega}{50\Omega + 175\Omega} \cdot 5V = 3.\bar{8}V$$

TASK 2 C




The value of U_X(t) and U_Y(t) stays constant between changes, because the reflection over the line takes t_d amount of time. See diagram of lecture:




$$V_e = \frac{R_T - Z_0}{R_T + Z_0} = \frac{175\Omega - 75\Omega}{175\Omega + 75\Omega} = 0.4$$

$$r_b = \frac{R_I - Z_0}{R_I + Z_0} = \frac{50\Omega - 75\Omega}{50\Omega + 75\Omega} = -0.2$$

$$U_x(t) = U_y(t-1) + r_b \cdot [U_y(t-1) - U_x(t-2)]$$

$$U_y(t) = U_x(t-1) + V_e \cdot [U_x(t-1) - U_y(t-2)]$$

$U_x(0) = 3V$ (see Task 3A)

$U_y(1 \cdot t_d) = 3V + 0.4\,[3V - 0V] = 4.2V$

$U_x(2 t_d) = 4.2V + (-0.2)\,[4.2V - 3V] = 3.96V$

$U_y(3 \cdot t_d) = 3.96V + 0.4\,[3.96V - 4.2V] = 3.896V$

$U_x(4 \cdot t_d) = 3.8832V$

$U_y(5 \cdot t_d) = 3.89088V$

TASK 3 A

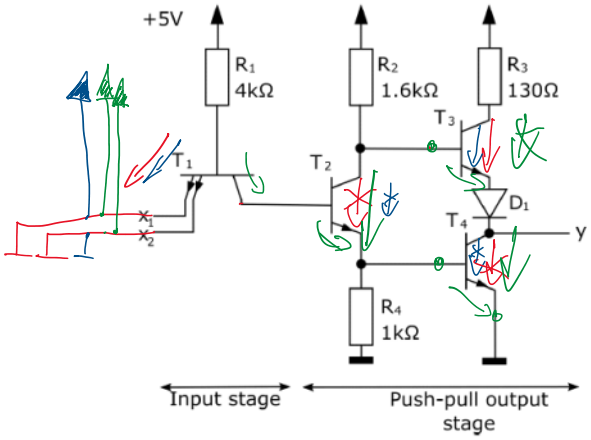



Figure 3.1: standard TTL output driver

| $x_1$ | $x_2$ | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $y$ |
|---|---|---|---|---|---|---|
| Low | Low | con. | non-con. | con. | non-con. | H |
| Low | High | con. | non-con. | con. | non-con. | H |
| High | Low | con. | non-con. | con. | non-con. | H |
| High | High | non-con. | con. | non-con. | con. | L |

Table 3.1: Logic Level

con. ≙ conducting
non-con. ≙ non-conducting

TASK 3 B

Advantages are e.g. 1. High currents are possible; 2. Little energy is consumed while static

These advantages hold true in comparison to other types e.g. RTL logic. CMOS for example consumes lower power.